MICROLINK 307x High Speed Scanning User Manual

Biodata Limited

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High Speed Scanning

The 3070 and 3071 modules control the sampling patterns of analogue input modules in a high speed scan. They are used in conjunction with a 304x A-D converter and one or more analogue input modules (305x, 306x). These other modules can be used in their normal slow mode even if a 307x is present.

9.1 3070—High Speed Scanning

You generally need to use the 3070 when sampling rates of more than a few tens of samples per second are required, or when accurate sample timings are required. Any number of analogue input channels can be scanned at high speed. The channels to be included in the scan are selected through software, along with the gain range for individual inputs. When scanning starts the system goes to the leftmost analogue input module and takes the first sample from the first channel included in the scan. The scan goes from left to right in module order and increasing channel number on each module. The 3070 maintains a count of channels scanned and returns to the first channel after the required number have been scanned.

Data acquisition may be started from a command sent out by software (a software trigger) or from a logic pulse derived from some external event (an external trigger). Which type of trigger is to be used is set from software.

You can disable the internal clock of the 3070, which controls the scan, using software. This will activate the external clock input. Now a scan is performed at each positive edge occurring at the clock input.

9.1.1 Operating Modes of the 3070

The 3070 can operate in 12 different modes, depending upon software settings.

Software Trigger

In modes 1, 2 and 3 sampling starts after a software trigger.

External Trigger

In modes 4, 5 and 6 sampling starts after an external trigger and further triggers will be ignored.

Multiple External Triggers

In modes 7, 8 and 9 sampling starts after an external trigger and continues for a specified number of scans. If a second trigger occurs

before the end of the specified count it will be ignored. If it occurs after the end of the count sampling will restart.

Level Controlled External Triggers: Gated Data Acquisition

In modes 10, 11 and 12 sampling will continue until either Trigger – is low or Trigger + is high. Sampling will then stop at the end of a complete scan.

Simple Multiplexing

In modes 1, 4, 7 and 10 all the enabled analogue input channels are sampled in turn.

Split Settling Time

In modes 2, 5, 8 and 11 one group of analogue channels is sampled at a different rate to a second group.

Dual Time Base

In modes 3, 6, 9 and 12 one group of analogue channels is sampled in every scan, whilst another group of channels is sampled only every nth scan. (May also be referred to as *dual scan rate*.)

9.1.2 Connection Notes

You only need to make connections to the 3070 when you use external triggers or clocks. All the other features set from software.

LEDs

Two front panel LEDs are provided in addition to the normal module (secondary) address LED. The HSC LED comes on whenever the High Speed Control bit of the mode register is set. It means that the 3070 is now controlling the 304x A-D converter and the analogue inputs. The TRIG LED comes on when the 3070 has been triggered. Normally the HSC LED will come on first and the TRIG LED some time later as determined by the trigger mode. Note that the TRIG LED may flash when the 3070 is setting up its sampling parameters.

Inputs

All inputs are TTL, 5 V CMOS compatible. They are pulled either high or low via 100K resistors so that if unused they may be left unconnected. Voltages applied should be restricted to the range 0-5 V.

Outputs

All outputs are TTL, 5 V CMOS compatible. They are capable of driving 10 LSTTL loads.

External Clock Inputs

There are 2 external clock inputs to accommodate positive and negative edge clocking. The External Clock + input is tied low by a 100K resistor. The External Clock – input is tied high by a 100K resistor. For positive edge clocking apply your signal to External Clock +. For negative edge clocking apply your signal to External Clock –. In both cases leave the unused input unconnected. Your clock pulse should be at least 1 msec wide. The active edge of the clock pulse causes a complete scan of the analogue channels. The channel rate and number of channels are controlled by the programmed settings of the 3070. Errors will occur if another clock pulse occurs before the previous scan is finished.

Trigger Inputs

There are 2 Trigger inputs to accommodate positive and negative edge triggering. The Trigger + input is tied low by a 100K resistor. The Trigger – input is tied high by a 100K resistor. For positive edge triggering apply your signal to Trigger +. For negative edge triggering apply your signal to Trigger –. In both cases leave the unused input unconnected. Your trigger pulse should be at least 1 μ sec wide. For details of triggering options see Section 9.1.1.

Trigger Out

The Trigger Out signal is high when the module is not triggered. It goes low when the unit is triggered and will stay low until sampling finishes. This falling edge can be used to trigger external events. In modes 7, 8, 9 it will return high at the end of the scan count. In modes 10, 11, 12 it will go low when sampling is possible and will be unaffected by the Trigger inputs.

Scan Rate

This pin produces a 1 μ sec wide pulse high at the start of each scan. It is included for diagnostic purposes.

Not HSC

This pin goes low whenever the 3070 is active and controlling sampling.

Mux Reset

This pin produces a 1 μ sec wide pulse high at the end of each scan when the multiplex is reset. It is included for diagnostic purposes.

Sample

This pin produces a 1 μ sec wide pulse high at each sample taken during a high speed scan. It is included for diagnostic purposes.

0 V and 5 V

The logic supply of the Microlink. The 5 V supply is short circuit protected.

Table 9.1 3070 High Speed Scanning Unit Pin Connections for 15-Way D Plug (Wiring View)

		8	External Clock +
External Clock –	15	7	Tringen
Trigger –	14	7	Trigger +
		6	unused
0 V	13	5	5 V
unused	12	-	
Scan Rate	11	4	unused
Scan Kale		3	unused
Trigger Out	10	0	Naturo
Mux Reset	9	2	Not HSC
		1	Sample

Please read the Connection Notes on the previous pages before making your connections.

9.2 3071—High Speed Digital Buffer

The 3071 provides a 16-bit wide digital input buffer. It can be used in one of three modes depending on how the front panel connector is wired.

- 1. Under 3070 control. The 3071 buffer is reset at the start of every 3070 controlled analogue scan. The digital inputs are sampled every time the 1st channel within an analogue scan is read. This is achieved by connecting First Sample to External Clock on the front panel connector.
- 2. Under external control. The 3071 buffer is cleared by a signal applied to Not Buffer Reset. Digital samples are taken every time a clock pulse occurs at the External Clock input. Both signals are supplied from an external source. In this mode there would be no 3070 module enabled within the Microlink.
- 3. Under mixed control. The 3071 buffer is reset internally at the start of every 3070 controlled analogue scan. However samples are taken at times determined by the rising edge of an external clock source connected to the External Clock input.

Data may be read at any time from the 3071 after 32 samples have been taken since the last request to Read. Reading data from the 3071 does not interfere with the collection process and no samples are lost during a read attempt.

Up to 16K samples of data can be stored before the buffer memory is full. Any attempt to store data after the buffer is full will not succeed and all attempts to read invalid data will be accompanied by an EOI signal. The EOI can only be cleared by resetting the buffer.

The current buffer volume status can be monitored by an optional extra LED module as a visual indication of how full the buffer is at any time. The minimum time between successive samples is 5 microseconds.

9.2.1 3071 Connection Notes

Input Voltages

The data bit inputs are TTL and 5 V CMOS compatible. Input voltages should not go outside the range 0–5 V. The 3900 Screw Terminal module can be used to mount components providing input protection or higher voltage inputs.

Inputs

"Not Buffer Reset" is pulled up to 5 V via a 100K resistor. A low level on Not Buffer Reset will clear the buffer and hold it reset until this input goes high.

"External Clock" is pulled down to 0 V via a 100K resistor. The data is sampled on a rising edge at this input. This input can be provided by an external TTL level signal or from the 3070 output "First Sample".

Outputs

The outputs are TTL and 5 V CMOS compatible. They are capable of driving 10 LSTTL loads.

"First Sample" gives an output pulse coincident with the first channel reading taken within every 3070 controlled analogue scan.

Linking "First Sample" to "External Clock" on the front panel connector will result in a sample being stored in the buffer simultaneously with the 1st channel read in any 3070 scan.

	07	19	0 V
+5 V	37	18	unused
unused	36	17	unused
unused	35	16	Bit 0 LSB 2nd byte
unused	34	15	Bit 1
unused	33		
unused	32	14	Bit 2
unused	31	13	Bit 3
unused	30	12	Bit 4
	29	11	Bit 5
unused		10	Bit 6
unused	28	9	Bit 7 MSB 2nd byte
unused	27	8	Bit 8 LSB 1st byte
Not Buffer Reset	26	7	Bit 9
unused	25	6	Bit 10
unused	24		
External Clock	23	5	Bit 11
First Sample	22	4	Bit 12
unused	21	3	Bit 13
unused	20	2	Bit 14
		1	Bit 15 MSB 1st byte

Table 9.2 3071 High Speed Digital Buffer Pin Connections for 37-Way D Plug (Wiring View)

Please read the Connection Notes before making your connections.

9.3 307x Specifications

9.3.1 3070 Scan Specifications

Module width	1		
Sample timings from	4 MHz quartz crystal		
Initial adjustment	±2 ppm		
Drift over temperature range 0–50°C	±50 ppm		
Scan rate	basic rate x multiplier		
basic rate	2 to 65535 in 0.25 μsec units		
multiplier	2 to 65535		
Channel rate (A, B)	2 to 65535 in 4 μ sec units		
Scan length A	1 to 32767		
Scan length B	0 to 32767		
Trigger pulse delay	1 to 65535 x 100 μsec		
Trigger output pulse length	= trigger pulse delay		

9.3.2 3071 Specifications

Buffer size

Minimum time between samples

32 Kbytes or 16 K 16-bit samples 4 μsec